WHAT IS CLAIMED IS:

1. A data output circuit comprising:

a multiplexer configured to receive a set of data bits and an output clock signal, wherein the set of data bits is received in a first order and the output clock signal is associated with one of a plurality of phases, and wherein the multiplexer is further configured to multiplex the set of data bits with the output clock signal to provide time multiplexed data bits in a second order; and

at least one output driver operatively coupled to the multiplexer and configured to receive and provide signal drive for the time multiplexed data bits.

2. The data output circuit of claim 1, further comprising:

a clock generator configured to receive an input clock signal and provide the output clock signal.

3. The data output circuit 2, wherein the clock generator includes

a delay lock loop circuit configured to provide a particular delay for the output clock signal.

4. The data output circuit 3, wherein the delay provided by the delay lock loop circuit is programmable.

5. The data output circuit of claim 1, wherein the phase of the output clock signal is selected based at least in part on an operating mode of the data output circuit.

6. A data output circuit comprising:

a first multiplexer configured to receive a set of data bits in a first order and provide the set of data bits in a second order;

data latches coupled to the first multiplexer and configured to receive and latch the set of data bits in the second order to provide a set of latched data bits; and

at least one output driver coupled to the data latches and configured to receive and provide signal drive for the set of latched data bits.

7. The data output circuit of claim 6, where the first multiplexer in configured to receive one or more pairs of data bits associated with even and odd memory addresses and provide one or more corresponding pairs of data bits for first and second temporal order to be provided from the at least one output driver.

8. The data output circuit of claim 7, where one of the even and odd memory addresses is received and the other address is generate internally.

9. The data output circuit of claim 8, where the even and odd memory addresses are consecutively numbered.

10. The data output circuit of claim 6, further comprising:

a second multiplexer coupled to the data latches and configured to receive and multiplex the set of latched data bits to provide time multiplexed data bits, and

wherein the at least one output driver is configured to receive and provide signal drive for the time multiplexed data bits.

11. The data output circuit of claim 10, wherein the data latches or the second multiplexer, or both, is operable to provide the time multiplexed data bits based on a clock signal having an adjustable phase.

12. The data output circuit of claim 11, further comprising:

a delay lock loop circuit configured to provide the clock signal having the adjustable phase.

13. The data output circuit of claim 10, wherein the data latches are operable to latch the set of data bits in the second order with a latch signal having a phase that is selected based on an operating mode of the data output circuit.

14. The data output circuit of claim 6, wherein the data latches comprise

a set of latches configured to latch the set of data bits in the second order with a latch signal.

15. The data output circuit of claim 14, wherein the latch signal is related to an input clock signal provided for clocking out data bits.

16. The data output circuit of claim 15, wherein the latch signal is delayed relative to the input clock signal by a selectable amount based on an operating mode of the data output circuit.

17. The data output circuit of claim 6, wherein the data latches comprise

a set of registers configured to register the set of data bits in the second order with a data read clock signal.

18. The data output circuit of claim 17, wherein the data read clock signal is generate based on one of a plurality of clock signals depending on an operating mode of the data output circuit.

19. The data output circuit of claim 18, wherein the data read clock signal is further delayed by an amount depending on the operating mode of the data output circuit.

20. The data output circuit of claim 6, wherein the data latches comprise

a set of latches configured to latch the set of data bits in the second order with a latch signal, and

a set of registers configured to register the set of data bits from the set of latches with a data read clock signal.

21. The data output circuit of claim 6, wherein the set of data bits in the first order is provided from a memory array based on a falling edge of an input clock signal.

22. The data output circuit of claim 6, wherein each of the at least one output driver is configured to receive and provide signal drive for the time multiplexed data bits, and wherein at least a subset of the at least one output driver can each be individually enabled and disabled to provide variable drive capability.

23. The data output circuit of claim 22, wherein the at least one output driver can be disabled to place the data output circuit in a tri-state condition.

24. The data output circuit of claim 6, and operable in a double data rate (DDR) write operation wherein two data bits are received, ordered, latched, and provided from the at least one output driver for each active clock cycle.

25. An integrated circuit comprising a plurality of data output circuits of claim 6.

26. A DRAM device comprising at least 32 data output circuits of claim 6, one data output circuit for each device data pin.

27. A data output circuit for use in a memory device comprising:

a first multiplexer configured to receive even and odd sequences of data bits and provide first and second sequences data bits, wherein the even sequence includes data bits prefetched from memory cells having even addresses and the odd sequence includes data bits prefetched from memory cells having odd addresses, and wherein the first sequence includes data bits to be provided from the data output circuit on a first clock phase and the second sequence includes data bits to be provided on a second clock phase;

a first set of latches coupled to the first multiplexer and configured to latch the first and second sequences data bits with a latch signal;

a second set of latches coupled to the first set of latches and configured to latch the sequences from the first set of latches with a data read clock signal;

a second multiplexer coupled to the second set of latches and configured to receive and multiplex the sequences of latched data bits to provide a sequence of time multiplexed data bits, and

at least one output driver coupled to the second multiplexer and configured to receive and provide signal drive for the sequence of time multiplexed data bits.

28. A data input circuit comprising:

a demultiplexer configured to receive and demultiplex a sequence of time multiplexed data bits into a plurality of sequences of data bits;

a multiplexer coupled to the demultiplexer and configured to receive and order the plurality of sequences of data bits to provide a plurality of ordered sequences; and

a plurality of driver circuits coupled to the multiplexer, each driver circuit configured to receive a respective sequence of data bits from the multiplexer and drive a respective data line.

29. The data input circuit of claim 28, wherein the sequence of time multiplexed data bits includes two data bits per active cycle of an input clock signal, and wherein the plurality of sequences of data bits include a first sequence and a second sequence, the first sequence including data bits corresponding to a first phase of the input clock signal and the second sequence including data bits corresponding to a second phase of the input clock signal.

30. The data input circuit of claim 29, wherein the multiplexer is configured to receive and order the first and second sequences to provide an even sequence and an odd sequence, the even sequence including data bits corresponding to memory cells having even addresses and the odd sequence including data bits corresponding to memory cells having odd addresses.

31. The data input circuit of claim 28, wherein the demultiplexer includes

a first set of latches configured to receive and latch the sequence of time multiplexed data bits with a plurality of phases of a latch signal to provide the plurality of sequences of data bits.

32. The data input circuit of claim 31, wherein the latch signal is generated from a DQS signal indicative of presence of valid data.

33. The data input circuit of claim 31, further comprising:

a second set of latches configured to receive and latch the plurality of ordered sequences with a data write clock signal, and

wherein the plurality of driver circuits couple to the second set of latches and are configured to receive respective sequences of data bits from the second set of latches and drive respective data lines.

34. A data input circuit for use in a memory device comprising:

a demultiplexer configured to receive and demultiplex a sequence of time multiplexed data bits into first and second sequences of data bits, wherein the first sequence includes data bits from the sequence of time multiplexed data bits that are associated with a first clock phase and the second sequence includes data bits from the sequence of time multiplexed data bits that are associated with a second clock phase;

a multiplexer coupled to the demultiplexer and configured to receive the first and second sequences of data bits and provide even and odd sequences of data bits, wherein the even sequence includes data bits to be provided to memory cells having even addresses and the odd sequence includes data bits to be provided to memory cells having odd addresses;

a set of latches coupled to the multiplexer and configured to receive and latch the even and odd sequences of data bits with a data write clock signal; and

a plurality of driver circuits coupled to the set of latches, each driver circuit configured to receive a respective sequence of data bits from the set of latches and drive a respective data line.

35. A memory unit comprising:

decoding circuitry configured to receive address information and generate a set of control signals;

at least one memory array coupled to the decoding circuitry and configured to provide a plurality of sets of data values in response to the set of control signals;

conditioning circuitry coupled to the at least one memory array and configured to receive and condition the plurality of sets of data values to provide a plurality of sets of data bits; and

a plurality of output circuits coupled to the conditioning circuitry, each output circuit configured to receive a respective set of data bits and drive a respective data line, each output circuit including

a first multiplexer configured to receive and order the respective set of data bits,

data latches coupled to the first multiplexer and configured to receive and latch the set of ordered data bits, and

at least one output driver coupled to the data latches and configured to receive the set of latched data bits and drive the respective data line.

36. A method for providing a plurality of data bits to an output node in a multi data rate operation, the method comprising:

receiving a set of data bits in a first order;

ordering the set of data bits in the first order to provide the set of data bits in a second order;

data latching the set of data bits in the second order to provide a set of latched data bits; and

providing the set of latched data bits to the output node.

37. The method of claim 36, further comprising:

multiplexing the set of latched data bits into a sequence of time multiplexed data bits.

38. The method of claim 36, wherein the set of data bits in the first order corresponds to even and odd memory addresses and the set of data bits in the second order corresponds to first and second temporal order to be provided to the output node.

39. The method of claim 36, wherein the data latching includes

first latching the set of data bits in the second order with a latch signal to provide a set of first latched data bits.

40. The method of claim 39, wherein the data latching further includes

second latching the set of first latched data bits with a data read clock signal to provide a set of second latched data bits.

41. The method of claim 39, wherein the data read clock signal is generate based on one of a plurality of clock signals depending on a particular operation mode.

42. The method of claim 40, wherein the data latching further includes third latching one data bit in the set of second latched data bits with a signal related to the data read clock signal to provide a set of time aligned data bits.

43. The method of claim 36, wherein the set of latched data bits are provided to the output node with variable drive strength.

44. A method for providing a plurality of data bits to a memory array in a multi data rate operation, the method comprising:

receiving a sequence of time multiplexed data bits;

demultiplexing the sequence of time multiplexed data bits into a plurality of sequences of data bits;

ordering the plurality of sequences of data bits to provide a plurality of ordered sequences of data bits; and

providing the plurality of ordered sequences of data bits to the memory array.

45. The method of claim 44, wherein the demultiplexing includes:

first latching the sequence of time multiplexed data bits with a plurality of phases of a latch signal to generate the plurality of sequences of data bits.

46. The method of claim 44, further comprising:

second latching the plurality of ordered sequences of data bits with a data write clock signal to generate a plurality of sequences of latched data bits.

47. The method of claim 44, wherein the sequence of time multiplexed data bits includes two data bits per active cycle of an input clock signal, and wherein the plurality of sequences of data bits include a first sequence and a second sequence, the first sequence including data bits corresponding to a first phase of the input clock signal and

the second sequence including data bits corresponding to a second phase of the input clock signal.

48. The method of claim 47, wherein the ordering includes

selecting either the first or second sequence as an even sequence to be provided to even-numbered address memory cells, and

selecting the other second or first sequence as an odd sequence to be provided to odd-numbered address memory cells.